

IN THE CLAIM

1 1. (Canceled)

1 2. (Currently Amended) The method of claim 15 4 wherein said step of
2 forming said interconnect assembly comprises forming said interconnect assembly on a
3 releasable substrate.

1 3. (Currently Amended) The method of claim 15 4 wherein said step of
2 forming said interconnect assembly comprises forming at least one test pad in an
3 interconnect layer, which at least one test pad can be accessed and electrically
4 connected on opposing sides of said at least one test pad.

1 4. (Previously Amended) The method of claim 3 wherein said step of
2 forming at least one test pad forms a test pad having gold on a conductive field metal.

1 5. (Previously Amended) The method of claim 3 wherein said step of
2 forming said interconnect assembly comprises forming at least one test pad in a
3 plurality of stacked interconnect layers, each of which at least one test pad in each
4 interconnect layer can be accessed and electrically connected on opposing sides of
5 said at least one test pad

1 6. (Previously Amended) The method of claim 5 wherein said step of
2 forming at least one test pad in said plurality of stacked interconnect layers forms at
3 least one test pad in each layer having gold on a conductive field metal.

1 7. (Currently Amended) The method of claim 15 4 where said step of
2 forming said plurality of conductive bumps connected to the terminals of the integrated
3 circuit chip forms a metallic bump making connection to a terminal on said integrated
4 circuit chip and a solder layer disposed on said metallic bump.

1 8. (Previously Amended) The method of claim 7 wherein said step of
2 forming said interconnect assembly comprises forming at least one test pad in an
3 interconnect layer, which at least one test pad can be accessed and electrically
4 connected on opposing sides of said test pad, and wherein said step of bonding said
5 interconnect assembly to said pre-formed integrated circuit chip flip bonds said solder
6 layer onto one side of said test pad.

1 9. (Currently Amended) The method of claim 15 4 where said step of
2 passivating said bonded interconnect assembly and said pre-formed integrated circuit
3 chip into said integral structure to provide said electronic package comprises underfilling
4 said pre-formed integrated circuit chip with an insulating material to remove all voids
5 between said pre-formed prepared integrated circuit chip and said interconnect
6 assembly.

1 10. (Currently Amended) The method of claim 15 4 where said step of
2 passivating said bonded interconnect assembly and said pre-formed integrated circuit
3 chip into said integral structure to provide said electronic package comprises potting
4 said interconnect assembly and said pre-formed integrated circuit chip into an integral
5 package.

1 11. (Currently Amended) The method of claim 9 where said step of
2 passivating said bonded interconnect assembly and said pre-formed integrated circuit
3 chip into said integral structure to provide said electronic package comprises potting
4 said interconnect assembly and said pre-formed integrated circuit chip into an integral
5 package.

1 12. (Previously canceled)

1 13. (Previously Amended) The method of claim 10 further comprising a step
2 of accessing said pre-formed integrated circuit chip through electrical connection to at
3 least one test pad through a surface thereof opposing said surface of said at least one
4 test pad contacting a terminal of said pre-formed integrated circuit chip to test said pre-
5 formed integrated circuit chip.

1 14. (Currently Amended) The method of claim 10 further comprising a
2 plurality of interconnect assembly and pre-formed integrated circuit chips wherein said

3 interconnect assembly and pre-formed integrated circuit chips are bonded together to
4 form a corresponding plurality of electronic packages and further comprising the step of
5 releasing said plurality of electronic packages from each other.

1 15.(Currently Amended) A method of preparing a pre-formed integrated circuit
2 chip for encapsulation in an electronic package, comprising the steps of:
3 forming an interconnect assembly separately from said pre-formed integrated
4 circuit chip;
5 forming a plurality of conductive bumps connected to the terminals of the pre-
6 formed integrated circuit chip;
7 bonding said interconnect assembly to said pre-formed integrated circuit chip;
8 passivating said bonded interconnect assembly and said pre-formed integrated
9 circuit chip into an integral structure; and
10 thinning said pre-formed integrated circuit chip to provide said electronic
11 package,
12 the ~~The~~ method of ~~claim 1~~ further comprising a plurality of interconnect
13 assembly and pre-formed integrated circuit chips wherein said plurality of interconnect
14 assembly and pre-formed integrated circuit chips are bonded together to form a
15 corresponding plurality of electronic packages and further comprising the step of testing
16 said interconnect assembly and bonding a tested interconnect assembly in said step of
17 bonding said interconnect assembly to said pre-formed integrated circuit chip only if
18 said interconnect assembly tested good.

1 16. (Previously Amended) The method of claim 15 where said step of forming
2 said plurality of interconnect assemblies comprises forming said interconnect
3 assemblies simultaneously in a wafer and where said plurality of pre-formed integrated
4 circuit chips are individually bump bonded to successfully tested ones of said
5 interconnect assemblies.

1 17 - 33. (Canceled)

1 34. (Currently Amended) The method of claim 43 33 wherein the at least one
2 test pad has gold on a conductive field metal.

1 35. (Currently Amended) The method of claim 43 33 where said step of
2 forming said plurality of conductive bumps connected to the terminals of the integrated
3 circuit chip forms a metallic bump making connection to a terminal on said integrated
4 circuit chip and a solder layer disposed on said metallic bump.

1 36. The method of claim 35 wherein said step of forming said interconnect
2 assembly comprises forming at least one test pad in an interconnect layer, which at
3 least one test pad can be accessed and electrically connected on opposing sides of
4 said test pad, and wherein said step of bonding said interconnect assembly to said pre-
5 formed integrated circuit chip flip bonds said solder layer onto one side of said test pad.

1 37 – 39 (Canceled)

1 40. (Currently Amended) The method of claim 43 39 further comprising the
2 step thinning said pre-formed integrated circuit chip.

1 41. (Currently Amended) The method of claim 43 39 further comprising a step
2 of accessing said pre-formed integrated circuit chip through electrical connection to at
3 least one test pad through a surface thereof opposing said surface of said at least one
4 test pad contacting a terminal of said pre-formed integrated circuit chip to test said pre-
5 formed integrated circuit chip.

1 42. (Canceled)

1 43. (Currently Amended) A method of preparing a pre-formed integrated
2 circuit chip for encapsulation in an electronic package, comprising the steps of:
3 forming an interconnect assembly separately from said pre-formed integrated
4 circuit chip, said forming an interconnect assembly including the step of:
5 forming at least one test pad in a plurality of stacked interconnect layers,
6 each of which at least one test pad in each interconnect layer can be
7 accessed and electrically connected on opposing sides of said at least
8 one test pad;

9 forming a plurality of conductive bumps connected to the terminals of the pre-
10 formed integrated circuit chip;
11 bonding said interconnect assembly to said pre-formed integrated circuit chip;
12 and
13 passivating said bonded interconnect assembly and said pre-formed integrated
14 circuit chip into an integral structure to provide said electronic package,
15 where said step of passivating said bonded interconnect assembly and said pre-
16 formed integrated circuit chip into said integral structure to provide said electronic
17 package comprises underfilling said pre-formed integrated circuit chip with an insulating
18 material to remove all voids between said pre-formed integrated circuit chip and said
19 interconnect assembly,
20 where said step of passivating said bonded interconnect assembly and said pre-
21 formed integrated circuit chip into said integral structure to provide an electronic
22 package comprises potting said interconnect assembly and said pre-formed integrated
23 circuit chip into said integral package,
24 The the method of claim 39 further comprising a plurality of interconnect
25 assembly and pre-formed integrated circuit chips wherein said plurality of interconnect
26 assembly and pre-formed integrated circuit chips are bonded together to form a
27 corresponding plurality of electronic packages and further comprising the step of testing
28 said interconnect assembly and bonding a tested interconnect assembly in said step of
29 bonding said interconnect assembly to said pre-formed integrated circuit chip only if
30 said interconnect assembly tested good.

1 44. The method of claim 43 where said step of forming said plurality of
2 interconnect assemblies comprises forming said interconnect assemblies
3 simultaneously in a wafer and where said plurality of pre-formed integrated circuit chips
4 are individually bump bonded to successfully tested ones of said interconnect
5 assemblies.